(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 601 590 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
12.04.2000 Bulletin 2000/15

(51) Int. Cl.[7]: **G11C 11/40**, H01L 27/108

(21) Application number: **93119902.0**

(22) Date of filing: **09.12.1993**

(54) Semiconductor memory cell

Halbleiterspeicherzelle

Cellule de mémoire à semi-conducteurs

(84) Designated Contracting States:
DE FR GB

(30) Priority: **10.12.1992 JP 35220092**
07.05.1993 JP 13013093
07.09.1993 JP 24626493

(43) Date of publication of application:
15.06.1994 Bulletin 1994/24

(60) Divisional application:
99118869.9 / 0 971 360

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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor memory cell consisting of two transistors or one transistor formed by combining two transistors.

DESCRIPTION OF THE PRIOR ART

[0002] Fig. 12 shows a conventional dynamic memory cell consisting of a single transistor and a capacitor; the memory cell of this structure is generally known as a one-transistor memory cell and used as a semiconductor memory cell suitable for high density devices. In such a memory cell, the capacitance of the capacitor needs to be high enough to cause a voltage change on the associated bit line. However, the trend to smaller plan area of the semiconductor memory cell necessitates a reduction in the size of the capacitor formed in a horizontal plate-like shape, giving rise to the problem that when reading information stored as a charge on the memory cell capacitor, the information is masked by noise, or that, because of increasing stray capacitance on the bit line with each generation of memory cells, only a small voltage change can be caused to the bit line. In one approach to solving this problem, there is proposed a dynamic memory cell having a trench capacitor cell structure (see Fig. 13) or a stacked capacitor cell structure. However, because of processing limitations on how deep the trench can be formed and how high the stack (stacked layers) can be made, there is a limit to increasing the capacitance of the capacitor. Accordingly, it is said that dynamic memory cells of these structures encounter the limit of miniaturization in the dimensional region beyond the low submicron rule.

[0003] Furthermore, with transistors forming the semiconductor memory cells, reducing the transistor's plan area beyond the low submicron rule would introduce such problems as dielectric strength degradation, punch-through, etc., which would increase the possibility of leakage even under the rated voltage condition. With conventional transistor structures, therefore, it becomes difficult to ensure proper operation of the memory cell when the memory cell size is reduced.

[0004] To overcome the above limitations on the capacitance, there is proposed a memory cell structure wherein the memory cell is constructed with two transistors and the transistor channel current is sensed.

[0005] In the memory cell disclosed in Japanese Patent Unexamined Publication No. 63-19847, for example, a capacitor C_2 coupled to the gate and drain of a MOS transistor Q_1 is connected to a word line, as shown in Fig. 3 accompanying the same Patent Publication. Furthermore, the drain of the transistor Q_1 is connected to the gate of an SOI transistor Q_2 of the complementary type to the transistor Q_1. The drain of the transistor Q_2 is in turn connected to a fixed potential V_D, while the source of each of the transistors, Q_1 and Q_2, is connected to a bit line.

[0006] In the memory cell disclosed in the above Patent Publication, since the gate electrode of the SOI (silicon-on-insulator) transistor Q_2 is formed only on one principal surface side of the channel region thereof having two principal surfaces, an extra capacitor C_2 is needed to complete the structure of the memory cell. A further problem is that because of the charge or electric field applied (through an insulating film) to the other principal surface of the channel region of the SOI transistor Q_2, the operation of the SOI transistor Q_2 becomes unstable and it is difficult to reduce the channel length.

[0007] On the other hand, the memory cell disclosed in Japanese Patent Unexamined Publication No. 1-145850 is constructed with a write transistor 18, a read transistor 19 (an SOI transistor), and a protective diode 20, as shown in Fig. 1 accompanying the same Patent Publication. The source of the write transistor 18 is connected to the gate of the read transistor 19. The cathode of the protective diode 20 is connected to the drain of the read transistor 19. Further, the anode of the protective diode 20 and the drain of the write transistor 18 are connected to a bit line, while the source of the read transistor 19 and the gate of the write transistor 18 are connected to a word line.

[0008] In the memory cell disclosed in the above Patent Publication, since the read transistor 19 is an SOI transistor, when the source potential is caused to change to the same polarity as the gate potential (when writing a "1") the potential of the channel region changes with the change of the gate potential, resulting in an incomplete writing condition. It is therefore difficult to read the "1" with the expected certainty. Furthermore, in the read transistor 19, the gate electrode is formed only on one principal surface side of the channel region having two principal surfaces. Therefore, this structure also has the problem that because of the charge or electric field applied (through an insulating film) to the other principal surface side of the channel region of the read transistor 19, the operation of the read transistor 19 becomes unstable and it is difficult to reduce the channel length.

[0009] The memory cells disclosed in Japanese Patent Unexamined Publication Nos. 62-141693 and 62-254462 each comprise a write transistor T1, a read transistor T2, and a storage capacitor C, as shown in Fig. 1 accompanying the former Patent Publication. The drains of the transistors T1 and T2 are connected to a bit line, and the source of the

transistor T1 is connected to the storage capacitor and also to a first gate of the transistor T2. Further, the gate of the transistor T1 is connected to a write selection line, while a second gate (or a channel forming region such as a well) of the transistor T2 is connected to a read selection line.

[0010] When the read transistor T2 is formed from an SOI transistor, the first and second gates are respectively formed on the upper and lower surface sides of the channel region of the transistor T2 (refer to Japanese Patent Application No. 55-93521 and Japanese Patent Unexamined Publication No. 57-18364). This structure eliminates the problem that has placed a limitation on the reduction of the channel length. For the write transistor T1, on the other hand, only bulk-type transistors are disclosed as preferred embodiments, and therefore, there is a limit to the miniaturization of the memory cell as a whole. Furthermore, the structure requiring each word line to be divided into a read line and a write line has the problem of increased chip area or increased number of stacked layers.

[0011] The present invention is concerned with the structure of a memory cell constructed with two transistors and yet capable of solving the above enumerated problems. An object of the invention is to provide a semiconductor memory cell, a semiconductor memory cell for ASICs (Application Specific Integrated Circuits), and even a semiconductor memory cell with a single transistor formed by combining two transistors, of the structure that ensures stable transistor operation, that does not require the provision of a large-capacitance capacitor as required in prior art DRAMs, and that allows the channel length to be reduced and achieves miniaturization of the cell.

[0012] The JP 02097063 describes a memory cell wherein a first MOS transistor is formed on a primary face of a semiconductor substrate and a single crystal semiconductor layer is formed on the first MOS transistor with an insulating film interposed. In the single crystal semiconductor layer a second MOS transistor is formed provided with a gate electrode formed on a channel region which is sandwiched in between diffusion regions. The channel region of the second MOS transistor is arranged just above an impurity region of the impurity regions of the first MOS transistor and the thickness of a semiconductor layer of the second MOS transistor channel region is so set as to enable the channel region to be completely depleted when the second MOS transistor is in operation. The preamble of claim 1 is based in this document.

[0013] In the US 4330849 a semiconductor memory device is disclosed which comprises a semiconductor substrate having a first conductivity type, first and second regions of a second conductivity type opposite to said first type formed in the surface of the semiconductor substrate and separated by a certain space therebetween, a third region of the first conductivity type in the second region, and a gate electrode formed on an insulating film on the semiconductor substrate between the first and the third regions. By applying a gate voltage to the gate electrode charge carriers are transferred between the first and second regions in accordance with the data to be stored. The stored data is read out by applying a prescribed gate voltage to the gate electrode and by detecting the value of the current between the third region and the semiconductor substrate.

[0014] The JP 57002563 describes a memory device which is composed of an N-channel MOS transistor and a P-channel MOS transistor and an N-type electrode commonly used for both transistors and P-type electrode to which a reference potential is applied and which is also commonly used.

[0015] In a device as disclosed in the JP 01145850 a first MOS transistor is used for writing and holding data which have been written and stored in the gate electrode that also serves as a capacitor part in a second MOS transistor.

SUMMARY OF THE INVENTION

[0016] To achieve the above object there is provided a semiconductor memory cell, as indicated in claim 1. It comprises:

an information storage transistor TR_1 comprising a semiconductor channel layer Ch_1 having first and second opposing principal surfaces; first and second conductive gates, G_1 and G_2, respectively disposed opposite the two principal surfaces of the semiconductor channel layer Ch_1 with first and second barrier layer respectively interposed therebetween; and first and second conductive regions, L_1 and L_2, respectively connected to either end of the semiconductor channel layer Ch_1, and

a switching transistor TR_2 comprising a semiconductor channel forming region Ch_2 having a third principal surface; a third conductive gate G_3 disposed opposite the third principal surface of the semiconductor channel forming region Ch_2 with a third barrier layer interposed therebetween; and third and fourth conductive layers, L_3 and L_4, each formed in a surface region of the semiconductor channel forming region Ch_2 and near either end of the third conductive gate G_3, wherein

the fourth conductive layer L_4 is connected to the second conductive gate G_2,

the first conductive gate G_1 and the third conductive gate G_3 are connected to a first memory-cell-selection line,

the first conductive layer L_1 and the third conductive layer L_3 are connected to a second memory-cell-selection line,

the second conductive layer L_2 is connected to a fixed potential including zero potential, and

the semiconductor channel forming region Ch_2 is connected to a read/write selection line.

[0017] In the above structure, the conductive layers may be formed from a low-resistivity semiconductor, a silicide, a two-layered structure of silicide and semiconductor, a metal, or the like. The barrier layers serve as barriers to channel carriers, and may be formed from an insulating material or a wide-gap semiconductor material.

[0018] In one preferred mode of the semiconductor memory cell according to the first aspect of the invention, as shown in the schematic diagram of Fig. 4,

the information storage transistor TR_1 is formed from a transistor of a first conductivity type,
the switching transistor TR_2 is formed from a transistor of a conductivity type opposite to the first conductivity type,
the first conductive layer L_1 is connected to the second line via a fifth conductive layer L_5 which forms a rectifier junction with the first conductive layer L_1, and
the semiconductor channel forming region Ch_2 is connected to a second fixed potential including zero potential.

[0019] To achieve the above object, in accordance with a second aspect of the invention, there is provided a semiconductor memory cell, as shown in the schematic diagram of Fig. 7, comprising:

an information storage transistor TR_1 comprising a first semiconductor channel layer Ch_1 having first and second opposing principal surfaces; first and second conductive gates, G_1 and G_2, respectively disposed opposite the two principal surfaces of the first semiconductor channel layer Ch_1 with first and second barrier layers respectively interposed therebetween; and first and second conductive regions, L_1 and L_2, each connected to either end of the first semiconductor channel layer Ch_1, and
a switching transistor TR_2 comprising a second semiconductor channel layer Ch_2 having third and fourth opposing principal surfaces; third and fourth conductive gates, G_3 and G_4, respectively disposed opposite the two principal surfaces of the second semiconductor channel layer Ch_2 with third and fourth barrier layers respectively interposed therebetween; and third and fourth conductive layers, L_3 and L_4, each connected to either end of the second semiconductor channel region Ch_2, wherein
the fourth conductive layer L_4 is connected to the second conductive gate G_2,
the first conductive gate G_1 and the third conductive gate G_3 are connected to a first memory-cell-selection line,
the first conductive layer L_1 and the third conductive layer L_3 are connected to a second memory-cell-selection line,
the second conductive layer L_2 is connected to a fixed potential including zero potential, and
the fourth conductive gate G_4 is connected to a read/write selection line.

[0020] In one preferred mode of the semiconductor memory cell according to the second aspect of the invention, as shown in the schematic diagram of Fig. 10,

the information storage transistor TR_1 is formed from a transistor of a first conductivity type,
the switching transistor TR_2 is formed from a transistor of a conductivity type opposite to the first conductivity type,
the first conductive layer L_1 is connected to the second line via a fifth conductive layer L_5 which forms a rectifier junction with the first conductive layer L_1, and
the fourth conductive gate G_4 is connected to a second fixed potential including zero potential.

[0021] In the semiconductor memory cell of the present invention, one conductive gate of the information storage transistor and one conductive gate of the switching transistor are connected to the first memory-cell-selection line. The first memory-cell-selection line, therefore, need not be provided more than one, and the chip area can be reduced.

[0022] In the semiconductor memory cell of the first and second aspects of the present invention, the fourth conductive layer is connected to the second conductive gate. When writing information, the switching transistor conducts, and the information is stored in the form of a potential or charge on the second conductive gate of the information storage transistor. The threshold voltage of the information storage transistor required at the first conductive gate, when reading information, varies depending on the potential or charge (information) stored on the second conductive gate. This is because the space-charge regions overlap across the channel layer near the first and second gates. Therefore, when reading information, the operation of the information storage transistor can be controlled by applying an appropriately selected potential to the first conductive gate. Information reading is accomplished by sensing the operating condition (for example, magnitude of the channel current) of the information storage transistor.

[0023] In the information storage transistor, a conductive gate is provided opposite each of the two principal surfaces of the semiconductor channel layer. This structure stabilizes the operation of the information storage transistor and facilitates short-channel transistor design. This also eliminates the need for a large capacitor as required in prior art DRAMs.

[0024] The gate threshold voltage of the switching transistor is controlled by the potential applied to the read/write selection line. When writing information, the switching transistor is turned on in order to store the potential or charge on

the second conductive gate, and when the write operation is completed, it is turned off. The stored information is retained as a potential or charge on the second conductive gate until the information is read out.

[0025] In the semiconductor memory cell according to the second aspect of the present invention, the switching transistor has the fourth conductive gate. This serves to further stabilize the operation of the switching transistor. This is achieved by applying to the read/write selection line a signal for putting the switching transistor in an off condition without fail during information read operation.

[0026] When writing information, the first line is set at a potential high enough to turn on the switching transistor, and the capacitor between the regions SC_1 and SC_3 of the switching transistor is charged depending on the potential on the second line. As a result, the information is stored in the channel forming region (the second semiconductor region SC_3) of the information storage transistor in the form of a charge or a potential difference from the region SC_1.

[0027] When reading information, the region SC_1 is supplied with a read potential, and the potential or charge (information) stored in the channel forming region of the information storage transistor is converted to a charge or a potential difference between the second semiconductor region SC_3, which corresponds to the channel forming region Ch_1, and the second conductive region SC_4, which corresponds to a source/drain region. The threshold voltage of the information storage transistor required at the conductive gate varies depending on the charge (information). Therefore, the on/off operations of the information storage transistor can be controlled, when reading information, by applying an appropriately selected potential to the conductive gate. Information reading is accomplished by sensing the operating condition of the information storage transistor.

[0028] In the semiconductor memory cell of the invention, the stored information is retained in the form of a potential, potential difference, or charge, but since the stored information decays with time because of leakage currents due to junction leaks, etc., refreshing is necessary, and the memory cell operates in the same manner as other DRAM cells.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029]

Fig. 1 is a diagram showing the principle of operation of a semiconductor memory cell according to a first aspect of the present invention.

Fig. 2 is a schematic cross-sectional view of a portion of a semiconductor memory cell according to Embodiment 1 of the present invention.

Fig. 3 is a diagram showing a modified example of Embodiment 1.

Fig. 4 is a diagram showing the principle of operation of a semiconductor memory cell according to a preferred mode of the first aspect of the invention.

Fig. 5 is a schematic cross-sectional view of a portion of a semiconductor memory cell according to Embodiment 2 of the present invention.

Fig. 6 is a diagram showing a modified example of Embodiment 2.

Fig. 7 is a diagram showing the principle of operation of a semiconductor memory cell according to a second aspect of the present invention.

Fig. 8 is a schematic cross-sectional view of a portion of a semiconductor memory cell according to Embodiment 3 of the present invention.

Fig. 9 is a diagram showing a modified example of Embodiment 3.

Fig. 10 is a diagram showing the principle of operation of a semiconductor memory cell according to a preferred mode of the second aspect of the present invention.

Fig. 11 is a schematic cross-sectional view of a portion of a semiconductor memory cell according to Embodiment 4 of the present invention.

Fig. 12 is a conceptual diagram showing a prior art one-transistor memory cell.

Fig. 13 is a cross-sectional view of a memory cell having a prior art trench capacitor cell structure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] The semiconductor memory cell of the invention will be described below in accordance with preferred embodiments thereof.

EMBODIMENT 1

[0031] Embodiment 1 is concerned with a semiconductor memory cell according to a first aspect of the invention. The semiconductor memory cell, the principle of operation of which is shown in Fig. 1 and cross sections of a portion of which are shown schematically in Figs. 2 and 3, comprises an information storage transistor TR_1 and a switching

transistor TR_2.

[0032] The information storage transistor TR_1 comprises a semiconductor channel layer Ch_1, a first conductive gate G_1, a second conductive gate G_2, and first and second conductive layers, L_1 and L_2, each connected to either end of the semiconductor channel layer Ch_1. The switching transistor TR_2 comprises a semiconductor channel forming region Ch_2, a third conductive gate G_3, and third and fourth conductive layers, L_3 and L_4, each formed in the surface area of the semiconductor channel forming region Ch_2 in contacting relationship forming a rectifier junction therewith. The third conductive gate G_3 is formed in such a manner as to bridge the third conductive layer L_3 and the fourth conductive layer L_4.

[0033] The semiconductor channel layer Ch_1 has two opposing principal surfaces, the first principal surface MS_1 and the second principal surface MS_2. The first conductive gate G_1 is formed opposite the principal surface MS_1 of the semiconductor channel layer with a first barrier layer BL_1 interposed therebetween. Likewise, the second conductive gate G_2 is formed opposite the principal surface MS_2 of the semiconductor channel layer with a second barrier layer BL_2 interposed therebetween. The semiconductor channel forming region Ch_2 has a third principal surface MS_3. The third conductive gate G_3 is formed opposite the third principal surface MS_3 of the semiconductor channel forming region Ch_2 with a third barrier layer BL_3 interposed therebetween.

[0034] The fourth conductive layer L_4 is connected to the second conductive gate G_2. The first conductive gate G_1 and the third conductive gate G_3 are connected to a first memory-cell-selection line (for example, a word line). In the structural example shown in Fig. 2, the first conductive gate G_1 and the third conductive gate G_3 are common. The first conductive layer L_1 and the third conductive layer L_3 are connected to a second memory-cell-selection line (for example, a bit line). The second conductive layer L_2 is connected to a fixed potential including zero potential. The semiconductor channel forming region Ch_2 is connected to a read/write selection line. The read/write selection line may be a common well or a substrate. In Embodiment 1, a common well is used. The second memory-cell-selection line (for example, a bit line) need not be provided more than one, and the chip area can be reduced.

[0035] The conductive layers may be formed from a low-resistivity semiconductor, a silicide, a two-layered structure of silicide and semiconductor, a metal or the like. The barrier layers serve as barriers to channel carriers, and may be formed from an insulating material or a wide-gap semiconductor material.

[0036] In Embodiment 1, the information storage transistor TR_1 has an SOI structure. That is, with the multilayered structure shown in Fig. 2, the total area that the information storage transistor and the switching transistor take up can be made approximately equal to the area that one transistor takes up, thus allowing the chip area to be reduced.

[0037] The operation of the semiconductor memory cell will be described below, taking for example a case in which the information storage transistor TR_1 and the switching transistor TR_2 are both n-type transistors.

[0038] Potentials applied to the various lines for a memory write are designated as follows:

First memory-cell-selection line (e.g., word line) : V_W
Second memory-cell-selection line (e.g., bit line) "0" write : V_0
"1" write : V_1
Read/write selection line : V_{B_W}

[0039] Potentials applied to the various lines for a memory read are designated as follows. Note that during a read cycle, the read/write selection line is reverse biased.

First memory-cell-selection line (e.g., word line) : V_R
Read/write selection line : V_{B_R}

[0040] For read/write, the fixed potential to which the second conductive layer L_2 is connected is designated as follows:

Fixed potential to which the second conductive layer L_2 is connected : V_2

[0041] The threshold voltages of the information storage transistor TR_1 required at the first conductive gate G_1 for memory read/write operations are designated as follows:

"0" read/write : V_{TH1_0}
"1" read/write : V_{TH1_1}

[0042] The potential of the second conductive gate G_2 is different between a "0" read/write and a "1" read/write. As a result, the threshold voltage of the information storage transistor TR_1 required at the first conductive gate G_1 differs between a "0" read/write and a "1" read/write. The information storage transistor TR_1 is provided with two conductive

gates, G_1 and G_2, on opposite sides of the semiconductor channel layer Ch_1; this structure serves to stabilize the operation of the information storage transistor TR_1, and facilitates short-channel design. Furthermore, a capacitor having as large capacitance as required in prior art DRAMs is not required.

[0043] The threshold voltage of the switching transistor TR_2 required at the third conductive gate G_3 for a write operation is designated as V_{TH2_W}. Further, the threshold voltage of the switching transistor TR_2 required at the third conductive gate G_3 for a read operation is designated as V_{TH2_R}. The threshold voltage of the switching transistor TR_2 required at the third conductive gate G_3 is different between memory write and memory read because the potential applied to the read/write selection line differs between write and read operations.

[0044] The relationships between the various potentials are set as follows:

$$|V_W| > |V_{TH2\_W}|$$

$$|V_{TH1\_0}| > |V_R| > |V_{TH1\_1}|$$

$$|V_{TH2\_R}| > |V_R|$$

[0045] The operation of the semiconductor memory cell of Embodiment 1 will be described below.

Information write

[0046] When writing information "0" (second line potential: V_0) or "1" (second line potential: V_1), the potential of the first line is V_W. Therefore, the potential at the third conductive gate G_3 of the switching transistor TR_2 is also V_W. Since the potential of the read/write selection line is V_{B_W}, the threshold voltage, V_{TH2_W}, of the switching transistor TR_2 required at the third conductive gate has the following relationship with respect to V_W.

$$|V_W| > |V_{TH2\_W}|$$

As a result, the switching transistor TR_2 is ON. Therefore, the potential at the second conductive gate G_2 of the information transistor TR_1 is V_0 (when writing information "0") or V_1 (when writing information "1").

[0047] When writing information, the potential at the first conductive gate G_1 of the information storage transistor TR_1 is V_W. The threshold voltage of the information storage transistor TR_1 required at the first conductive gate G_1 is V_{TH1_0} or V_{TH1_1}. If the relationship

$$|V_W| > |V_{TH1\_0}| > |V_{TH1\_1}|$$

exists between these potentials, the information storage transistor TR_1 is also ON, but writing is performed whether the information storage transistor TR_1 is ON or OFF.

[0048] As described above, when writing information "0" or "1", the potential at the second conductive gate G_2 of the information storage transistor TR_1 is V_0 or V_1. That is, the second conductive gate G_2 is held at a potential corresponding to the information "0" or "1", and this condition is substantially maintained within a prescribed time until the information is read out. During the information retention period after the information is written and before the information is read out, the various portions of the information storage transistor TR_1 and the switching transistor TR_2 are set at such potentials that neither transistor will conduct.

Information read

[0049] When reading information "0" or "1", the potential of the first line is V_R. Therefore, the potential at the third conductive gate G_3 of the switching transistor TR_2 is V_R. Since the potential of the read/write selection line is V_{B_R}, a reverse bias is applied between the source and the channel forming region of the switching transistor TR_2. V_{B_R} is set so that the threshold voltage, V_{TH2_R}, of the switching transistor TR_2 required at the third conductive gate has the following relationship with respect to V_R.

$$|V_{TH2\_R}| > |V_R|$$

The switching transistor TR_2 is thus held OFF.

[0050] When reading information, the potential at the first conductive gate G_1 of the information storage transistor TR_1 is V_R. The threshold voltage of the information storage transistor TR_1 at the first conductive gate G_1 is V_{TH1_0} or V_{TH1_1}. The threshold voltage of the information storage transistor TR_1 is dependent on the potential of the second con-

ductive gate G_2. The following relationship exists between these potentials.

$$|V_{TH1\_0}| > |V_R| > |V_{TH1\_1}|$$

Therefore, when the stored information is "0", the information storage transistor TR_1 is OFF. On the other hand, when the stored information is "1", the information storage transistor TR_1 is ON.

[0051] Thus, the information storage transistor TR_1 is set to an ON or OFF condition, depending on the stored information. Therefore, when the stored information is "1", current flows to the second line; when the stored information is "0", no current but the leakage current flows to the second line. The stored information can be read in this manner by the information storage transistor TR_1.

[0052] The above-described operating conditions of the information storage transistor TR_1 and the switching transistor TR_2 are summarized in Table 1. The potential values given in Table 1 are only illustrative examples, and each potential can take any value as long as it satisfies the above conditions.

Table 1

Unit: volts

Memory write	"0" write		"1" write	
1st line potential	V_W	2.0	V_W	2.0
2nd line potential	V_0	0	V_1	1.0
Read/write line		V_{B-W}		V_{B-W}
Threshold of TR_2 required at 3rd gate	V_{TH2-W}	0.5	V_{TH2-W}	0.5
3rd gate potential	V_W	2.0	V_W	2.0
Condition of TR_2	ON		ON	
2nd gate potential	V_0	0	V_1	1.0
Threshold of TR_1 required at 1st gate	V_{TH1-0}	1.1	V_{TH1-1}	0.5
1st gate potential	V_W	2.0	V_W	2.0
condition of TR_1	ON		ON	
Memory read	"0" read		"1" read	
1st line potential	V_R	1.0	V_R	1.0
Read/write line		V_{B-R}		V_{B-R}
Threshold of TR_2 required at 3rd gate	V_{TH2-R}	1.5	V_{TH2-R}	1.5
3rd gate potential	V_R	1.0	V_R	1.0
Condition of TR_2	OFF		OFF	
2nd gate potential	V_0	0	V_1	1.0
Threshold of TR_1 required at 1st gate	V_{TH1-0}	1.1	V_{TH1-1}	0.5
1st gate potential		1.0		1.0
Condition of TR_2	OFF		ON	
Fixed potential	V_2	0	V_2	0
2nd line current	OFF		ON	

[0053] A modified example of the semiconductor memory cell of Embodiment 1 illustrated in Fig. 2 is shown schematically in cross section in Fig. 3. In the semiconductor memory cell shown in Fig. 2, the first conductive gate G_1 and the third conductive gate G_3 are common. By contrast, in the semiconductor memory cell shown in Fig. 3, the second conductive gate G_2 and the fourth conductive layer L_4 are common. Also, the read/write selection line is formed from a

well. While a slightly larger plan area is required as compared with the memory cell shown in Fig. 2, the memory cell shown in Fig. 3 have the advantages of relatively smooth surface topography, which is advantageous in lithography, and a less number of contacts.

EMBODIMENT 2

[0054] Embodiment 2 is concerned with a preferred mode of the semiconductor memory according to the first aspect of the invention. The semiconductor memory cell, the principle of operation of which is shown in Fig. 4 and cross sections of a portion of which are shown schematically in Figs. 5 and 6, comprises an information storage transistor TR_1 and a switching transistor TR_2. The structures of the information storage transistor TR_1 and the switching transistor TR_2 are fundamentally the same as those of Embodiment 1, except for the points hereinafter described.

[0055] The information transistor TR_1 is formed from a transistor of a first conductivity type, for example, a p-type transistor, and the switching transistor TR_2 is formed from a transistor of the opposite conductivity type to that of the information storage transistor TR_1, for example, an n-type transistor. In this case, if the first conductive layer L_1 and the second conductive layer L_2 are formed from semiconductor material, then their conductivity type should be p type. Likewise, if the first conductive gate G_1, the second conductive gate G_2, the third conductive gate G_3, the third conductive layer L_3, and the fourth conductive layer L_4 are formed from semiconductor material, then their conductivity type should be n^+ type. Alternatively, these regions may be formed from a silicide, a two-layer structure of silicide and semiconductor, or a metal. The semiconductor channel forming region Ch_2 is connected to a second fixed potential including zero potential.

[0056] Further, the first conductive layer L_1 is connected to the second line via a fifth conductive layer L_5 which forms a rectifier junction with the first conductive layer. The provision of the fifth conductive layer serves to prevent without fail a current from flowing into the information storage transistor TR_1 during the writing of information. Furthermore, there is no possibility of the information write voltage being applied to the information storage transistor TR_1 and thereby interfering with the write operation as was the case with the prior art.

[0057] The operation of the semiconductor memory cell of Embodiment 2 will be described below.

[0058] The potentials of the information storage transistor TR_1 and the switching transistor TR_2 are set to satisfy the following relationships.

$$|V_W| > |V_{TH2\_W}|$$

$$|V_{TH1\_1}| > |V_R| > |V_{TH1\_0}|$$

Information write

[0059] When writing information "0" (second line potential: V_0) or "1" (second line potential: V_1), the potential of the first line is V_W (>0). Therefore, the potential at the third conductive gate G_3 of the switching transistor TR_2 is also V_W (>0). Since the second fixed potential is V_{B_W}, if V_W is set as

$$|V_W| > |V_{TH2\_W} + V_0 \text{ or } V_1|$$

where V_{TH2_W} is the threshold voltage of the switching transistor TR_2 required at the third conductive gate G_3, then the switching transistor TR_2 is ON. Therefore, the potential at the second conductive gate G_2 of the information transistor TR_1 is V_0 (when writing information "0") or V_1 (when writing information "1").

[0060] When writing information, the potential at the first conductive gate G_1 of the information storage transistor TR_1 is V_W (>0). Therefore, when V_0 or $V_1 < V_W - V_{TH1\_1}$, the information storage transistor TR_1 is OFF. Even if it is ON, current flow is blocked by the presence of the rectifier junction between the first conductive layer L_1 and the fifth conductive layer L_5.

[0061] As described above, when writing information "0" or "1", the potential at the second conductive gate G_2 of the information storage transistor TR_1 is V_0 or V_1. That is, the second conductive gate G_2 is held at a potential corresponding to the information "0" or "1", and this condition is substantially maintained until the information is read out. During the information retention period after the information is written and before the information is read out, the various portions of the information storage transistor TR_1 and the switching transistor TR_2 are set at such potentials that neither transistor will conduct.

Information read

[0062] When reading information "0" or "1", the potential of the first line is V_R (<0). Therefore, the potential at the

third conductive gate G_3 of the switching transistor TR_2 is V_R (<0), and the switching transistor TR_2 remains OFF unless the potential of the second line is made more negative than $V_R - V_{TH2\_R}$. Normally, for a read operation, the second line is set at a small potential and information is read by sensing the current.

[0063] The potential at the first conductive gate G_1 of the information storage transistor TR_1 is V_R (<0). The threshold voltage of the information storage transistor TR_1 required at the first conductive gate G_1 is V_{TH1_0} or V_{TH1_1}. The threshold voltage of the information storage transistor TR_1 is dependent on the potential of the second conductive gate G_2. The following relationship exists between these potentials.

$$|V_{TH1\_1}| > |V_R| > |V_{TH1\_0}|$$

Therefore, when the stored information is "0", the information storage transistor TR_1 is ON. On the other hand, when the stored information is "1", the information storage transistor TR_1 is OFF.

[0064] Thus, the information storage transistor TR_1 is set to an ON or OFF condition, depending on the stored information. The second conductive layer L_2 of the information storage transistor TR_1 is connected to the fixed potential (V_2); therefore, when the stored information is "0", current flows to the second line, and when the stored information is "1", current does not flow to the second line. The stored information can be read in this manner by the information storage transistor TR_1.

[0065] A cross section of a portion of the semiconductor memory cell of Embodiment 2 is shown schematically in Fig. 5. The semiconductor memory cell of Embodiment 2 is fundamentally the same as the semiconductor memory cell shown in Fig. 2, except that the information storage transistor TR_1 and the switching transistor TR_2 are of different conductivity types and that the first conductive layer L_1 is connected to the second line via the n-type fifth conductive layer L_5 which forms a rectifier junction with the p-type first conductive layer L_1.

[0066] Table 2 summarizes the operating conditions of the semiconductor memory cell in which the information storage transistor TR_1 is formed from a p-type transistor and the switching transistor TR_2 is formed from an n-type transistor.

Table 2

Unit: volts

Memory write	"0" write		"1" write	
1st line potential	V_W	1.5	V_W	1.5
2nd line potential	V_0	0	V_1	1.0
Read/write line		V_{B-W}		V_{B-W}
Threshold of TR_2 required at 3rd gate	V_{TH2-W}	0.5	V_{TH2-W}	0.5
3rd gate potential	V_W	1.5	V_W	1.5
Condition of TR_2	ON		ON	
2nd gate potential	V_0	0	V_1	1.0
1st gate potential	V_W	1.5	V_W	1.5
Condition of TR_1	OFF		OFF	
Memory read	"0" read		"1" read	
1st line potential	V_R	-1.0	V_R	-1.0
3rd gate potential	V_R	-1.0	V_R	-1.0
Condition of TR_2	OFF		OFF	
2nd gate potential	V_0	0	V_1	1.0
Threshold of TR_1 required at 1st gate	V_{TH1-0}	-0.5	V_{TH1-1}	-1.1
1st gate potential		-1.0		-1.0
Condition of TR_1	ON		OFF	
Fixed potential		V_2		V_2
2nd gate current	ON		OFF	

[0067] The potential values given in Table 2 are only illustrative examples, and each potential can take any value as long as it satisfies the above conditions.

[0068] A modified example of the semiconductor memory cell illustrated in Fig. 5 is shown schematically in cross section in Fig. 6. The semiconductor memory cell shown is fundamentally the same as the semiconductor memory cell shown in Fig. 3, except that the information storage transistor TR_1 and the switching transistor TR_2 are of different conductivity types and that the first conductive layer L_1 is connected to the second line via the n-type fifth conductive layer L_5 which forms a rectifier junction with the p-type first conductive layer L_1.

Embodiment 3

[0069] Embodiment 3 is concerned with a semiconductor memory cell according to a second aspect of the invention. The semiconductor memory cell, the principle of operation of which is shown in Fig. 7 and cross sections of a portion of which are shown schematically in Figs. 8 and 9, comprises an information storage transistor TR_1 and a switching transistor TR_2. The information storage transistor TR_1 comprises a first semiconductor channel layer Ch_1, a first conductive gate G_1, a second conductive gate G_2, and first and second conductive layers, L_1 and L_2, each connected to either end of the first semiconductor channel layer Ch_1. The switching transistor TR_2 comprises a second semiconductor channel layer Ch_2, a third conductive gate G_3, a fourth conductive gate G_4, and third and fourth conductive layers, L_3 and L_4, each connected to either end of the second semiconductor channel layer Ch_2. In Embodiment 3, the information storage transistor TR_1 and the switching transistor TR_2 both have an SOI structure (including a structure in which the barrier layer is formed from a wide-gap semiconductor, for example, GaAlAs as compared with GaAs).

[0070] The first semiconductor channel layer Ch_1 has two opposing principal surfaces, the first principal surface MS_1 and the second principal surface MS_2. The first conductive gate G_1 is formed opposite the principal surface MS_1

of the first semiconductor channel layer with a first barrier layer BL_1 interposed therebetween. Likewise, the second conductive gate G_2 is formed opposite the principal surface MS_2 of the first semiconductor channel layer with a second barrier layer BL_2 interposed therebetween.

[0071] The second semiconductor channel layer Ch_2 has two opposing principal surfaces, the third principal surface MS_3 and the fourth principal surface MS_4. The third conductive gate G_3 is formed opposite the third principal surface MS_3 of the second semiconductor channel layer Ch_2 with a third barrier layer BL_3 interposed therebetween. Likewise, the fourth conductive gate G_4 is formed opposite the fourth principal surface MS_4 of the second semiconductor channel layer Ch_2 with a third barrier layer BL_4 interposed therebetween.

[0072] The fourth conductive layer L_4 is connected to the second conductive gate G_2. In Embodiment 3, the fourth conductive layer L_4 and the second conductive gate G_2 are common. The first conductive gate G_1 and the third conductive gate G_3 are connected to a first memory-cell-selection line (for example, a word line). The first conductive layer L_1 and the third conductive layer L_3 are connected to a second memory-cell-selection line (for example, a bit line). The second conductive layer L_2 is connected to a fixed potential including zero potential. The fourth conductive gate G_4 is connected to a read/write selection line.

[0073] The semiconductor memory cell of Embodiment 3 is different from the semiconductor memory cell of Embodiment 1 in that the switching transistor TR_2 has the fourth conductive gate G_4. This serves to further stabilize the operation of the switching transistor TR_2 and yet allows further miniaturization.

[0074] When the information storage transistor TR_1 and the switching transistor TR_2 are both n-type transistors, the operation of the semiconductor memory cell is the same as that described in Embodiment 1 (see Table 1), and therefore, detailed explanation thereof is not repeated here.

[0075] A modified example of the semiconductor memory cell of Embodiment 3 illustrated in Fig. 8 is shown schematically in cross section in Fig. 9. In the semiconductor memory cell shown in Fig. 8, the second conductive gate G_2 and the fourth conductive layer L_4 are common. By contrast, in the semiconductor memory cell shown in Fig. 9, the first conductive gate G_1 and the third conductive gate G_3 are formed in the same substrate surface. The first conductive gate G_1 and the third conductive gate G_3 may be connected to each other. While a slightly larger plan area is required than that of the memory cell shown in Fig. 8, the memory cell shown in Fig. 9 has the advantage that the first semiconductor channel layer Ch_1 and the second semiconductor channel layer Ch_2 can be formed using a single high-quality semiconductor layer whereas two such layers are needed in the structure of the semiconductor memory cell shown in Fig. 8. There is a further advantage that the first conductive gate G_1 and the third conductive gate G_3 can be made common.

Embodiment 4

[0076] Embodiment 4 is concerned with a preferred mode of the semiconductor memory cell according to the second aspect of the invention. The semiconductor memory cell, the principle of operation of which is shown in Fig. 10 and a cross section of a portion of which is shown schematically in Fig. 11, comprises an information storage transistor TR_1 and a switching transistor TR_2. The structures of the information storage transistor TR_1 and the switching transistor TR_2 are fundamentally the same as those of Embodiment 3, except for the points hereinafter described.

[0077] The information transistor TR_1 is formed from a transistor of a first conductivity type, for example, a p-type transistor, and the switching transistor TR_2 is formed from a transistor of the opposite conductivity type to that of the information storage transistor TR_1, for example, an n-type transistor. In this case, if the first conductive layer L_1 and the second conductive layer L_2 are formed from semiconductor material, then their conductivity type should be p type. Likewise, if the first conductive gate G_1, the second conductive gate G_2, the third conductive gate G_3, the fourth conductive gate G_4, the third conductive layer L_3, and the fourth conductive layer L_4 are formed from semiconductor material, then their conductivity type should be n^+ type. The fourth conductive gate G_4 is connected to a second fixed potential including zero potential.

[0078] Further, the first conductive layer L_1 is connected to the second line via an n-type fifth conductive layer L_5 which forms a rectifier junction with the p-type first conductive layer L_1.

[0079] A cross section of a portion of the semiconductor memory cell of Embodiment 4 is shown schematically in Fig. 11. The semiconductor memory cell of Embodiment 3 is fundamentally the same as the semiconductor memory cell shown in Fig. 9, except that the first and second conductive layers, L_1 and L_2, are of different conductivity type and that the first conductive layer L_1 is connected to the second line via the n^+ fifth conductive layer L_5 which forms a rectifier junction with the p-type first conductive layer L_1. In Fig. 11, the fifth conductive layer L_5 and the rectifier junction between the first conductive layer L_1 and the fifth conductive layer L_5 are shown in schematic form for simplicity. It will also be appreciated that the first conductive gate G_1 and the third conductive gate G_3 may be connected to each other.

[0080] When the information storage transistor TR_1 is formed from a p-type transistor and the switching transistor TR_2 from an n-type transistor, the operation of the semiconductor memory cell is the same as that described in Embodiment 2 (see Table 2), and therefore, detailed explanation thereof is not repeated here.

Claims

1. A semiconductor memory cell comprising:

an information storage transistor (TR1) comprising a semiconductor channel layer (Ch_1) having first and second opposing principal surfaces (MS_1, MS_2); first and second conductive gates (G_1, G_2) respectively disposed opposite said two principal surfaces (MS_1, MS_2) of said semiconductor channel layer (Ch_1) with first and second barrier layers (BL_1, BL_2) respectively interposed therebetween; and first and second conductive regions (L_1, L_2) each connected to either end of said semiconductor channel layer (Ch_1), and
a switching transistor (TR_2) comprising a semiconductor channel forming region (Ch_2) having a third principal surface (MS_3); a third conductive gate (G_3) disposed opposite said third principal surface (MS_3) of said semiconductor channel forming region (Ch_2) with a third barrier layer (BL_3) interposed therebetween; and third and fourth conductive regions (L_3, L_4) each formed in a surface region of said semiconductor channel forming region (Ch_2) in contacting relationship forming a rectifier junction therewith, said third conductive gate (G_3) being formed in such a manner as to bridge said third conductive region (L_3) and said fourth conductive region (L_4), wherein
said fourth conductive region (L_4) is connected to said second conductive gate (G_2), characterized in that
said first conductive gate (G_1) and said third conductive gate (G_3) are connected to a first memory-cell-selection line (word line),
said first conductive layer (L_1) and said third conductive layer (L_3) are connected to a second memory-cell-selection line (bit line),
said second conductive layer (L_2) is connected to a fixed potential including zero potential, and
said semiconductor channel forming region (Ch_2) is connected to a read/write selection line.

2. A semiconductor memory cell according to claim 1, wherein

said information storage transistor (TR_1) is formed from a transistor of a first conductivity type,
said switching transistor (TR_2) is formed from a transistor of a conductivity type opposite to the first conductivity type,
said first conductive region (L1) is connected to said second line via a fifth conductive region (L5) which forms a rectifier junction with said first conductive region (L_1), and
said semiconductor channel forming region (Ch_2) is connected to a second fixed potential including zero potential.

3. A semiconductor memory cell according to claim 1 wherein

said switching transistor (TR_2) comprises a fourth conductive gate (G_4) disposed opposite said third conductive gate (G3) on a second principal surface (MS_4) of said second semiconductor channel layer (Ch_2) with a fourth barrier layer (BL_4) interposed therebetween;

said fourth conductive gate (G4) being connected to said read/write selection line instead of said semiconductor channel forming region (CH_2).

4. A semiconductor memory cell according to claim 3, wherein

said information storage transistor (TR_1) is formed from a transistor of a first conductivity type,
said switching transistor (TR_2) is formed from a transistor of a conductivity type opposite to the first conductivity type,
said first conductive layer (L_1) is connected to said second line via a fifth conductive layer (L_5) which forms a rectifier junction with said first conductive layer (L_1), and
said fourth conductive gate (G_4) is connected to a second fixed potential including zero potential.

Patentansprüche

1. Halbleiterspeicherzelle mit:

- einem Informationsspeichertransistor (TR_1) mit einer Halbleiterkanalschicht (Ch_1) mit einer ersten und einer zweiten Hauptfläche (MS_1, MS_2), die voneinander abgewandt sind; einem ersten und einem zweiten leitenden

Gate (G_1, G_2), die den beiden Hauptflächen (MS_1, MS_2) der Halbleiterkanalschicht (Ch_1) jeweils gegenüberstehend angeordnet sind, wobei eine erste bzw. eine zweite Barriereschicht (BL_1, BL_2) dazwischen eingefügt ist; und einem ersten und einem zweiten leitenden Bereich (L_1, L_2), von denen jeder mit einem Ende der Halbleiterkanalschicht (Ch_1) verbunden ist; und

- einem Schalttransistor (TR_2) mit einem einen Halbleiterkanal bildenden Bereich (Ch_2) mit einer dritten Hauptfläche (MS_3); einem dritten leitenden Gate (G_3), das der dritten Hauptfläche (MS_3) des den Halbleiterkanal bildenden Bereichs (Ch_2) gegenüberstehend angeordnet ist, wobei eine dritte Barriereschicht (BL_3) dazwischen eingefügt ist; und einem dritten und einem vierten leitenden Bereich (L_3, L_4), die jeweils in einem Oberflächenbereich des den Halbleiterkanal bildenden Bereichs (Ch_2) in kontaktierender Beziehung, wobei mit diesem ein Gleichrichterübergang gebildet ist, ausgebildet ist, wobei das dritte leitende Gate (G_3) auf solche Weise ausgebildet ist, dass es den dritten leitenden Bereich (L_3) und den vierten leitenden Bereich (L_4) überbrückt; wobei
- der vierte leitende Bereich (L_4) mit dem zweiten leitenden Gate (G_2) verbunden ist;

dadurch gekennzeichnet, dass

- das erste leitende Gate (G_1) und das dritte leitende Gate (G_3) mit einer ersten Speicherzelle-Auswählleitung (Wortleitung) verbunden sind;
- die erste leitende Schicht (L_1) und die dritte leitende Schicht (L_3) mit einer zweiten Speicherzelle-Auswählleitung (Bitleitung) verbunden sind;
- die zweite leitende Schicht (L_2) mit einem festen Potenzial, einschließlich dem Potenzial Null, verbunden ist; und
- der den Halbleiterkanal bildende Bereich (Ch_2) mit einer Lese/Schreib-Auswählleitung verbunden ist.

2. Halbleiterspeicherzelle nach Anspruch 1, bei der

- der Informationsspeichertransistor (TR_1) aus einem Transistor von erstem Leitungstyp besteht;
- der Schalttransistor (TR_2) aus einem Transistor von einem Leitungstyp entgegengesetzt zum ersten Leitungstyp besteht;
- der erste leitende Bereich (L_1) über einen fünften leitenden Bereich (L_5), der mit dem ersten leitenden Bereich (L_1) einen Gleichrichterübergang bildet, mit der zweiten Leitung verbunden ist; und
- der den Halbleiterkanal bildende Bereich (Ch_2) mit einem zweiten festen Potenzial, einschließlich dem Potenzial Null, verbunden ist.

3. Halbleiterspeicherzelle nach Anspruch 1, bei der

- der Schalttransistor (TR_2) ein viertes leitendes Gate (G_4) aufweist, das abgewandt vom dritten leitenden Gate (G_3) auf einer zweiten Hauptfläche (MS_4) der zweiten Halbleiterkanalschicht (Ch_2) ausgebildet ist, wobei dazwischen eine vierte Barriereschicht (BL_4) eingefügt ist;
- wobei das vierte leitende Gate (G_4) mit der Lese/Schreib-Auswählleitung statt mit dem den Halbleiterkanal bildenden Bereich (Ch_2) verbunden ist.

4. Halbleiterspeicherzelle nach Anspruch 3, bei der

- der Informationsspeichertransistor (TR_1) aus einem Transistor von erstem Leitungstyp besteht;
- der Schalttransistor (TR_2) aus einem Transistor von einem Leitungstyp entgegengesetzt zum ersten Leitungstyp besteht;
- die erste leitende Schicht (L_1) über eine fünfte leitende Schicht (L_5), die mit der ersten leitenden Schicht (L_1) einen Gleichrichterübergang bildet, mit der zweiten Leitung verbunden ist; und
- das vierte leitende Gate (G_4) mit einem zweiten festen Potenzial, einschließlich dem Potenzial Null, verbunden ist.

Revendications

1. Cellule de mémoire à semiconducteur comprenant :

un transistor de mémorisation d'informations (TR_1) comprenant une couche de canal à semiconducteur (Ch_1) présentant des première et seconde surfaces principales opposées (MS_1, MS_2), des première et seconde grilles conductrices (G_1, G_2) disposées respectivement à l'opposé desdites deux surfaces principales de ladite couche de canal à semiconducteur (Ch_1), des première et seconde couches de barrière (BL_1, BL_2) étant respectivement intercalées entre celles-ci, et des première et seconde régions conductrices, (L_1, L_2), chacune

étant reliée à l'une ou l'autre extrémité de ladite couche de canal à semiconducteur (Ch_1), et

un transistor de commutation (TR_2) comprenant une région de formation de canal à semiconducteur (Ch_2) présentant une troisième surface principale (MS_3), une troisième grille conductrice (G_3) disposée à l'opposé de ladite troisième surface principale (MS_3) de ladite région de formation de canal à semiconducteur (Ch_2), une troisième couche de barrière (BL_3) étant intercalée entre celles-ci, et des troisième et quatrième régions conductrices (L_3, L_4), chacune étant formée dans une région de surface de ladite région de formation de canal à semiconducteur (Ch_2) en relation de contact formant une jonction de redresseur avec celles-ci, ladite troisième grille conductrice (G_3) étant formée de telle manière qu'elle ponte ladite troisième région conductrice (L_3) et ladite quatrième région conductrice (L_4), dans laquelle

ladite quatrième région conductrice (L_4) est reliée à la seconde grille conductrice (G_2), caractérisée en ce que ladite première grille conductrice (G_1) et ladite troisième grille conductrice (G_3) sont reliées à une première ligne de sélection de cellule de mémoire (ligne de mot),

ladite première couche conductrice (L_1) et ladite troisième couche conductrice (L_3) sont reliées à une seconde ligne de sélection de cellule de mémoire (ligne de bit),

ladite seconde couche conductrice (L_2) est reliée à un potentiel fixe comprenant un potentiel zéro, et

ladite région de formation de canal à semiconducteur (Ch_2) est reliée à une ligne de sélection de lecture/écriture.

2. Cellule de mémoire à semiconducteur selon la revendication 1, dans laquelle

ledit transistor de mémorisation d'informations (TR_1) est formé à partir d'un transistor d'un premier type de conductivité,

ledit transistor de commutation (TR_2) est formé à partir d'un transistor d'un type de conductivité opposé au premier type de conductivité,

ladite première région conductrice (L_1) est reliée à ladite seconde ligne par l'intermédiaire d'une cinquième région conductrice (L_5) qui forme une jonction de redresseur avec la première région conductrice (L_1), et

ladite région de formation de canal à semiconducteur (Ch_2) est reliée à un second potentiel fixe comprenant un potentiel zéro.

3. Cellule de mémoire à semiconducteur selon la revendication 1, dans laquelle

ledit transistor de commutation comprend une quatrième grille conductrice (G_4) disposée à l'opposé de ladite troisième grille conductrice (G_3) sur une seconde surface principale (MS_4) de ladite seconde couche de canal à semiconducteur (Ch_2) avec une quatrième couche de barrière (BL_4) intercalée entre celles-ci,

ladite quatrième grille conductrice (G_4) étant reliée à ladite ligne de sélection de lecture/écriture au lieu de ladite région de formation de canal à semiconducteur (Ch_2).

4. Cellule de mémoire à semiconducteur selon la revendication 3, dans laquelle

ledit transistor de mémorisation d'informations (TR_1) est formé à partir d'un transistor d'un premier type de conductivité,

ledit transistor de commutation (TR_2) est formé à partir d'un transistor d'un type de conductivité opposé au premier type de conductivité,

ladite première couche conductrice (L_1) est reliée à ladite seconde ligne par l'intermédiaire d'une cinquième couche conductrice (L_5) qui forme une jonction de redresseur avec ladite première couche conductrice (L_1), et

ladite quatrième grille conductrice (G_4) est reliée à un second potentiel fixe comprenant un potentiel zéro.

FIG. 1

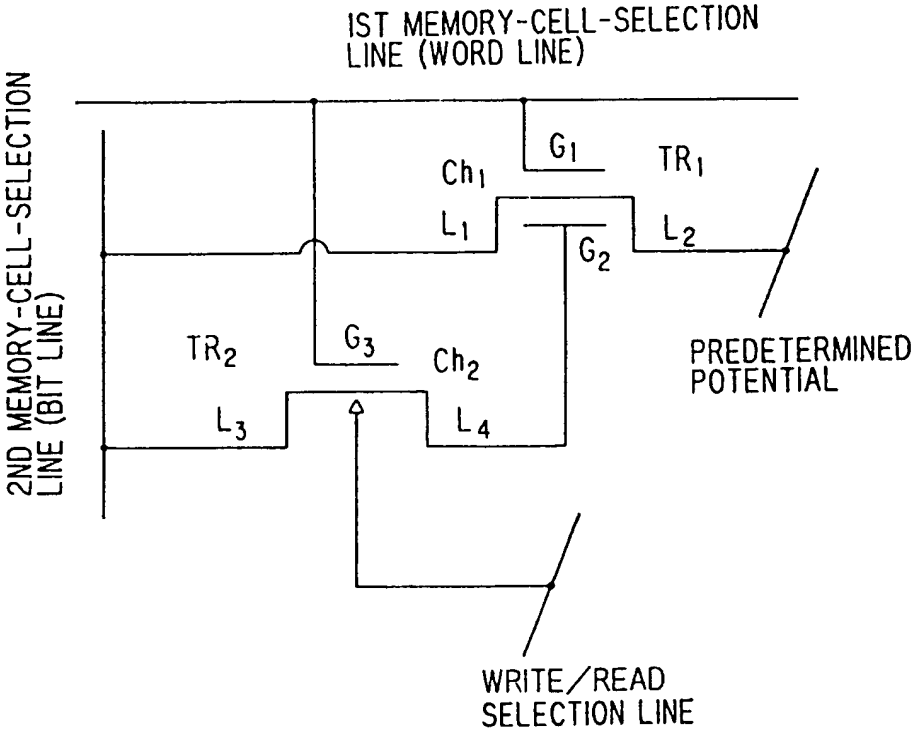
1ST MEMORY-CELL-SELECTION LINE (WORD LINE)
2ND MEMORY-CELL-SELECTION LINE (BIT LINE)
G1
TR1
Ch1
L1
L2
G2
TR2
G3
Ch2
L3
L4
PREDETERMINED POTENTIAL
WRITE/READ SELECTION LINE

FIG. 2

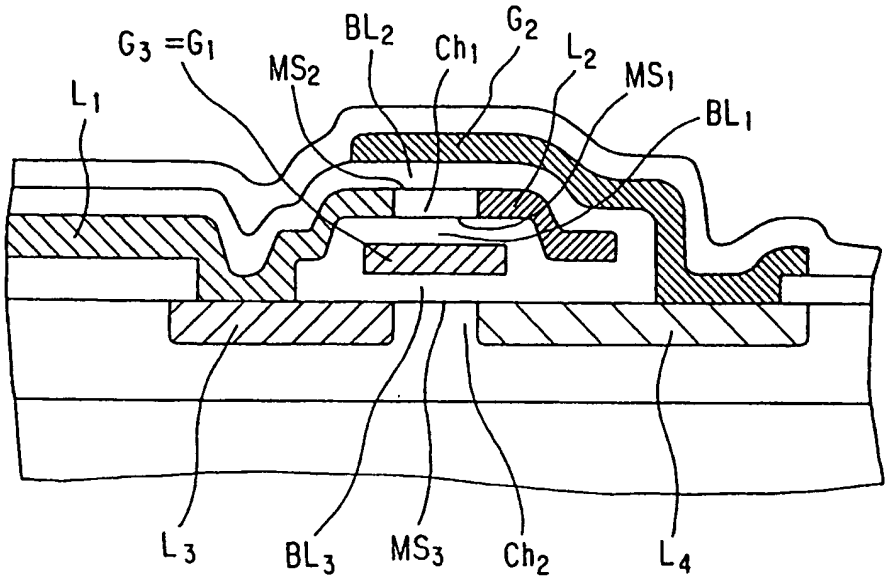
G3 =G1
BL2
Ch1
G2
L2
MS1
MS2
L1
BL1
L3
BL3
MS3
Ch2
L4

FIG. 3

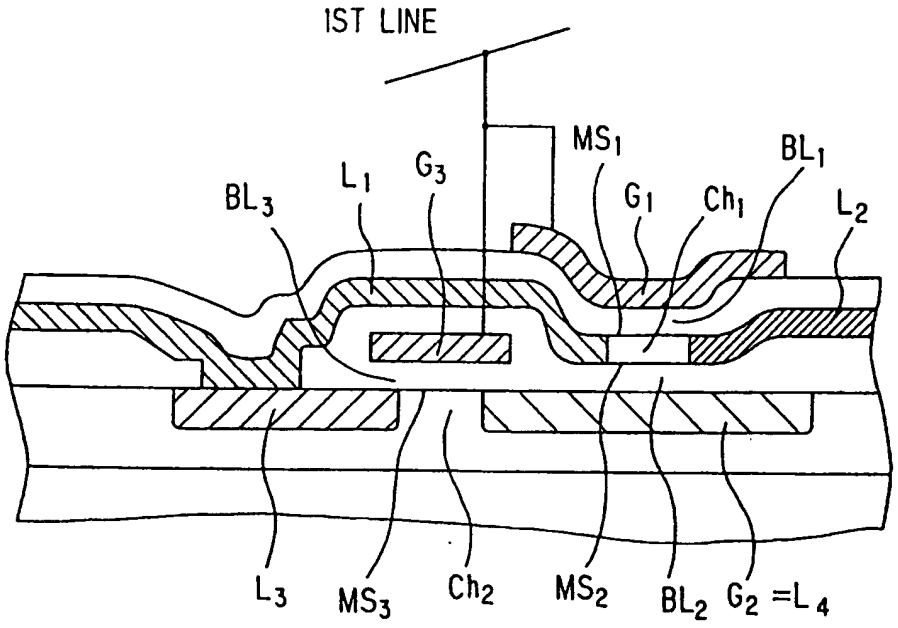
1ST LINE
MS1
BL1
L1
G3
BL3
G1
Ch1
L2
L3
MS3
Ch2
MS2
BL2
G2 =L4

FIG. 4

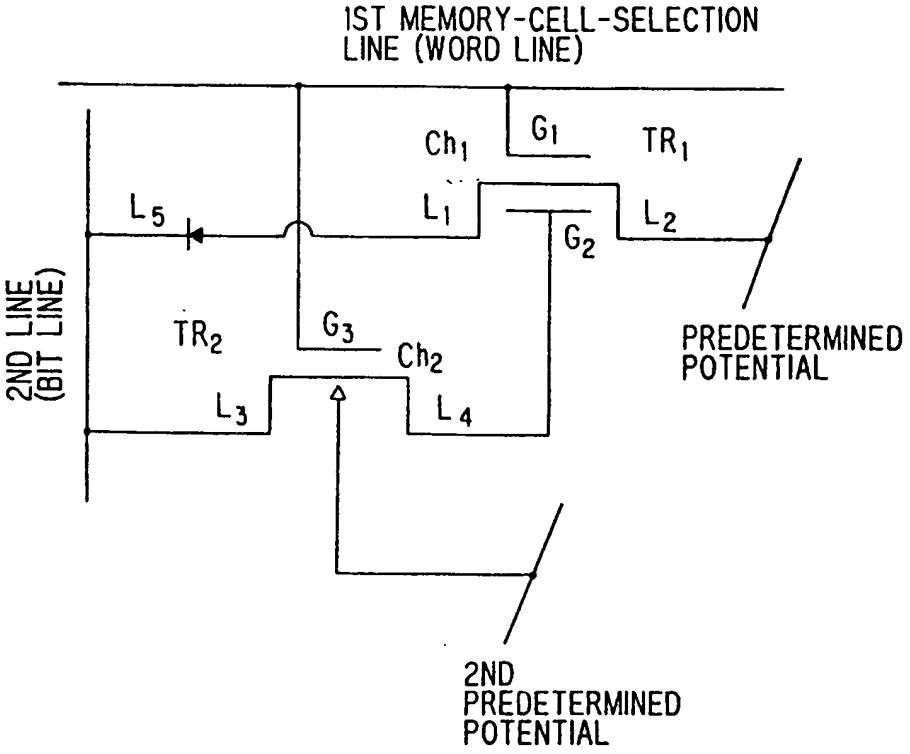
1ST MEMORY-CELL-SELECTION LINE (WORD LINE)
Ch1
G1
TR1
L5
L1
L2
G2
2ND LINE (BIT LINE)
TR2
G3
Ch2
L3
L4
PREDETERMINED POTENTIAL
2ND PREDETERMINED POTENTIAL

FIG.5

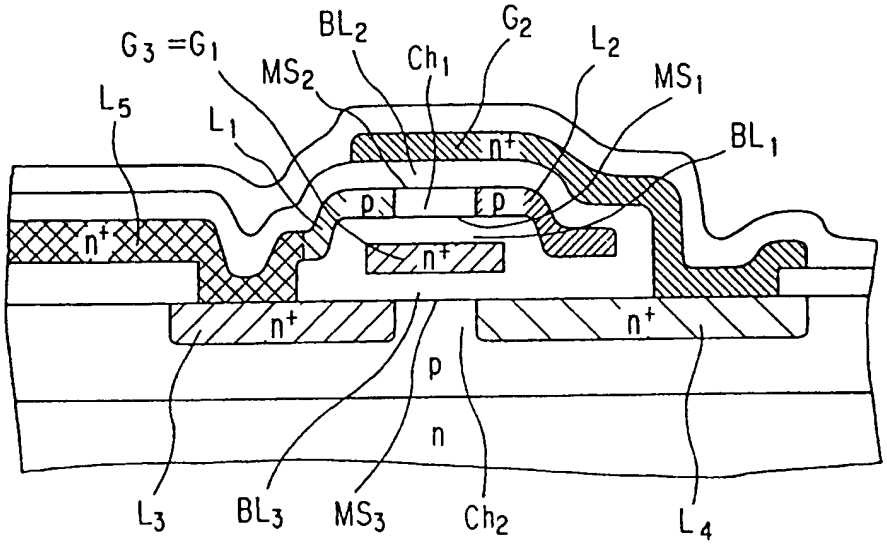
G3 =G1
BL2
G2
L2
MS2
Ch1
MS1
L5
L1
BL1
n+
p
p
n+
n+
n+
p
n
L3
BL3
MS3
Ch2
L4

FIG.6

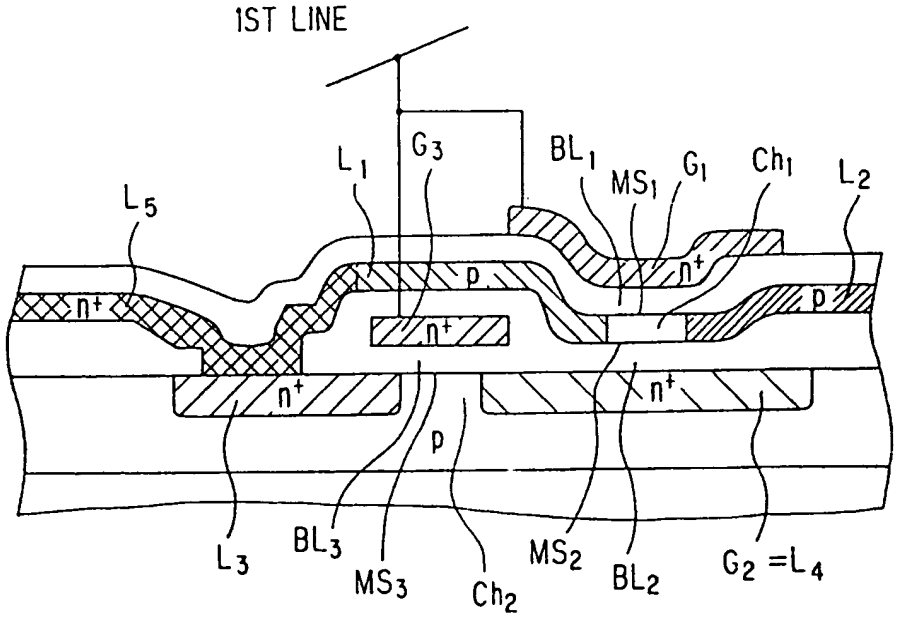
1ST LINE
L1
G3
BL1
MS1
G1
Ch1
L2
L5
n+
p
n+
p
n+
n+
p
L3
BL3
MS3
Ch2
MS2
BL2
G2 =L4

FIG. 7

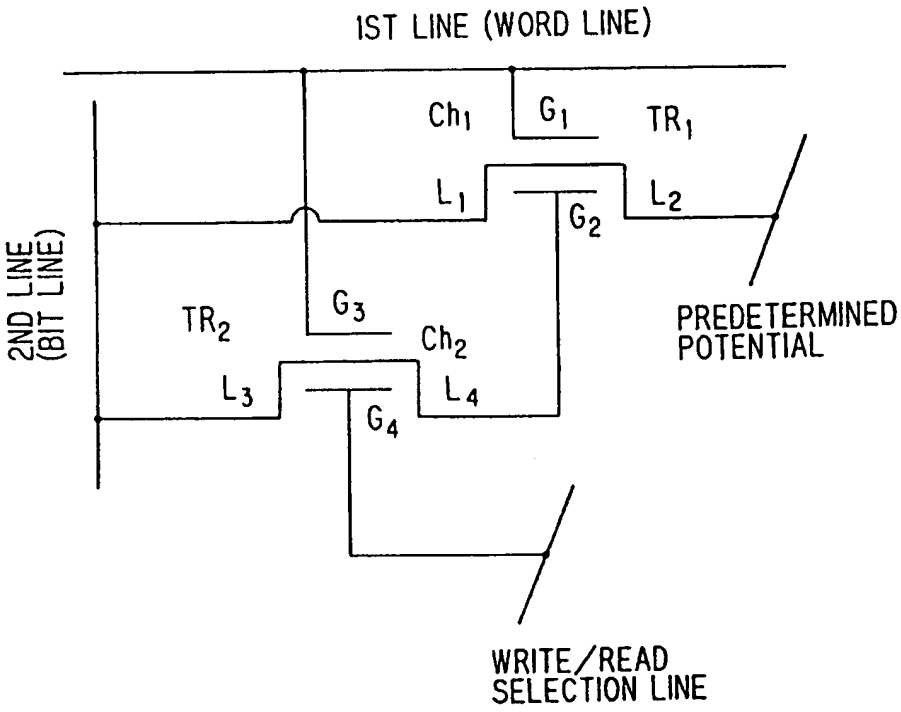
1ST LINE (WORD LINE)
Ch1
G1
TR1
L1
L2
G2
2ND LINE (BIT LINE)
TR2
G3
Ch2
L3
L4
G4
PREDETERMINED POTENTIAL
WRITE/READ SELECTION LINE

FIG. 8

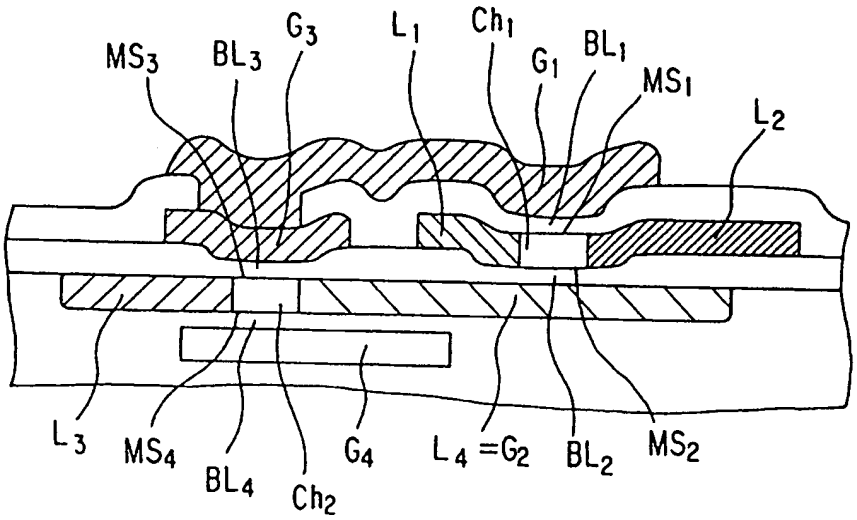
MS3
BL3
G3
L1
Ch1
G1
BL1
MS1
L2
L3
MS4
BL4
Ch2
G4
L4 =G2
BL2
MS2

FIG. 9

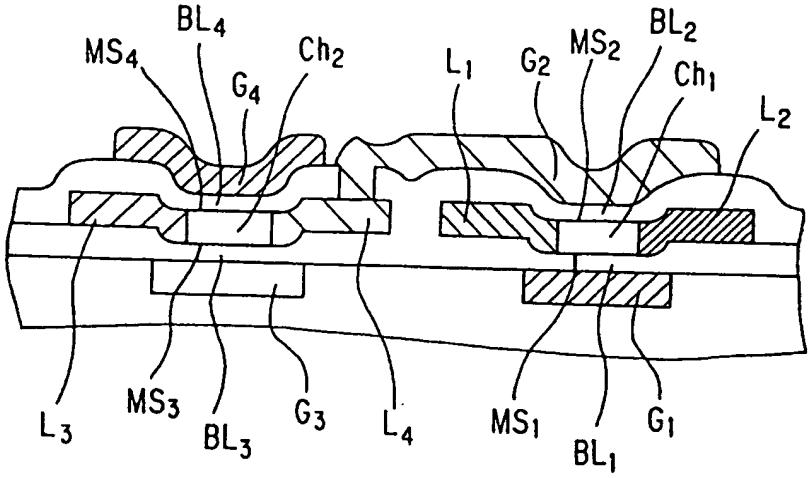
BL4
MS4
Ch2
G4
L1
G2
MS2
BL2
Ch1
L2
L3
MS3
BL3
G3
L4
MS1
BL1
G1

FIG. 10

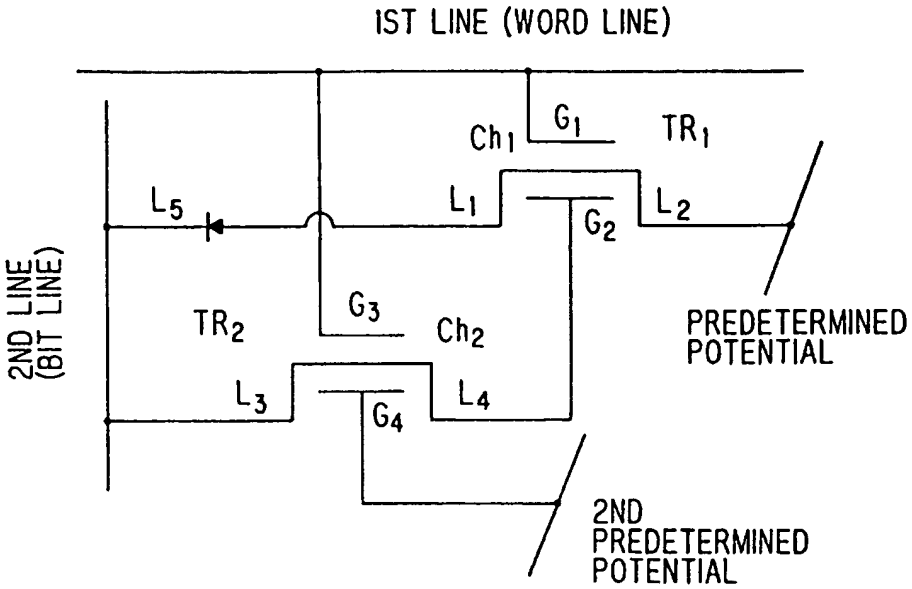
1ST LINE (WORD LINE)
2ND LINE (BIT LINE)
Ch1
G1
TR1
L5
L1
L2
G2
TR2
G3
Ch2
PREDETERMINED POTENTIAL
L3
G4
L4
2ND PREDETERMINED POTENTIAL

FIG. 11

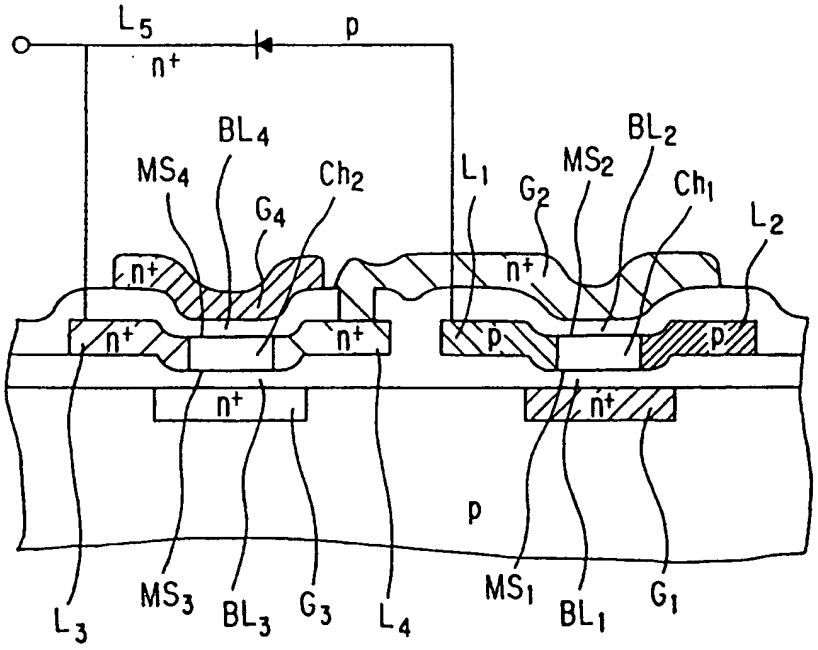
L5
p
n+
BL4
MS4
Ch2
G4
L1
G2
MS2
BL2
Ch1
L2
n+
n+
n+
p
p
n+
n+
p
L3
MS3
BL3
G3
L4
MS1
BL1
G1

FIG. 12 PRIOR ART

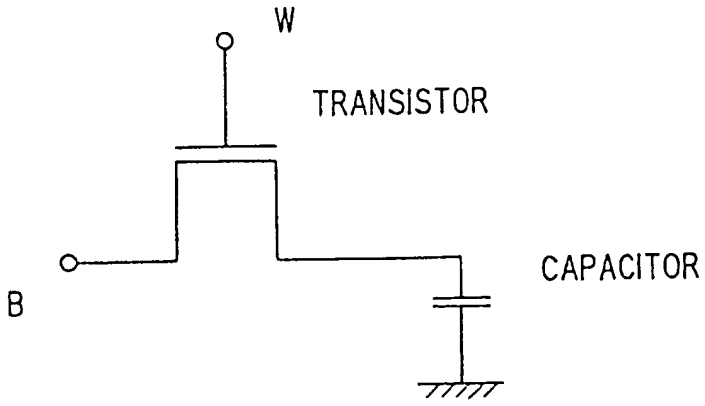

FIG. 13